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10/606,225	06/26/2003	Hideaki Watanabe	024016-00062	3762

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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,225	WATANABE, HIDEAKI	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2,4,13,14,16,19 and 20* is/are rejected.

7)☐ Claim(s) *3,5-12,15,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The indicated allowability of claims 1, 4-7, 10-13, and 16-19 is withdrawn in view of the newly discovered reference(s) to Sumi, US Patent No. 6,522,183. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Sumi, US Patent No. 6,522,183. All claim limitations disclosed in Sumi are shown in Figures 1-23.

Regarding claim 1, Sumi discloses a clock multiplying PLL circuit, comprising:

an oscillator circuit 112 for outputting an output clock signal;

first through n-th dividers (113-116) for dividing the output clock signal and thereby outputting first through n-th divided signals (FV11-FV14) (where n: an integer greater than or equal to 2) (column 6, lines 6-14), said first through n-th dividers being different in effective transition timings of the outputted first through n-th divided signals from one another (column 7, lines 5-19, line 66 – column 8, line 8);

a reference clock signal generating circuit 105 generating n types of first through n-th reference clock signals (FR11-FR14) different in phase from one another (column

5, line 56 – column 6, line 5) by using an input reference clock signal (output of 101); and

first through n-th phase comparators (106-109) for respectively comparing phases of the i-th reference clock signal and the i-th divided signals (where i: an integer 1 to n) (column 6, lines 15-65),

wherein an oscillation frequency of the output clock signal outputted from the oscillator circuit is changed based on the results of comparison by the first through n-th phase comparators (column 6, line 67 – column 7, line 4).

Regarding claim 2, Sumi further discloses the PLL circuit, wherein the first through n-th dividers respectively have the same dividing ratio 1/M (where M: an integer greater than or equal to 2) (column 6, lines 6-14, all feedback signal FV11-FV14 have an identical frequency, thus same dividing ratio, FIG. 3), and

when the number of pulses of the output clock signal outputted from the oscillator circuit is taken as P_j during a period from the effective transition timing of the first divided signal to the effective transition timing of the j-th divided signal (where j: an integer of 2 to n), a phase delay of the j-th reference clock signal when the first reference clock signal is set as the reference, is P_j/M cycles (column 7, line 45 – column 8, line 17, FIG. 3).

Regarding claim 4, Sumi further discloses the PLL circuit, wherein the first through n-th dividers respectively have the same dividing ratio 1/M (where M; an integer greater than or equal to 2) (column 6, lines 6-14, all feedback signal FV11-FV14 have an identical frequency, thus same dividing ratio, FIG. 3),

The number of pulses of an output clock signal outputted from the oscillator circuit is set as M.(j-1)/n during a period from the effective transition timing of the first divided signal to an effective transition timing of a j-th divided signal (where j: an integer of 2 to n) (column 7, line 45 – column 8, line 17, FIG. 3), and

a phase delay of a j-th reference clock signal when the first reference clock signal is set as the reference signal (column 7, lines 58-65).

Regarding claim 19, Sumi discloses a clock multiplying PLL circuit (FIG. 1) for PLL-controlling (column 7, line 45 – column 8, line 36) an oscillator circuit 112 and outputting an output clock signal F01 having multiplied frequency obtained by multiplying an input reference clock signal FR11 (column 7, line 58 – column 8, line 21), comprising:

n (where n: an integer greater than or equal to 2) dividers (113-116) having the same dividing ratio and for dividing the output clock signal (all feedback signal FV11-FV14 have an identical frequency, thus same dividing ratio, FIG. 3);

n-pieces of phase comparators (106-109) paired with the dividers (column 6, lines 15-65); and

a reference clock signal generating circuit 105 for generating n types of reference clock signals (FR11-FR14) different in phase from one another using the reference clock signal (column 5, line 55 – column 6, line 5),

wherein each of the phase comparators obtains a result of a phase comparison between each of the divided signals outputted from the dividers paired with the phase comparators and any of the n types of reference clock signals (column 6, lines 15-65), and the oscillator circuit is PLL-controlled by n-times of each cycle period of the

reference clock signal by the use of the result of phase comparison (column 7, line 45 – column 8, line 17).

Regarding claim 20, Sumi discloses a clock multiplying circuit (FIG. 1) for outputting an output clock signal F01 having multiplied frequency obtained by multiplying an input reference clock FR11 (column 7, line 58 – column 8, line 21), comprising:

an oscillating circuit 112; and

a multiple control circuit 117 for performing PLL-control on the oscillator circuit by a predetermined number of times greater than or equal to 2 for each cycle period of the reference clock signal (column 7, line 45 – column 8, line 17).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sumi, US Patent No. 6,522,183.

Regarding claims 13, 14, and 16, Sumi discloses the PLL circuit as per claims 1, 2, and 4, respectively. In addition, Sumi further discloses a reference signal generating means 105 having a plurality of delay elements 102-104 for generating delayed instances of the reference clock signal (column 5, lines 56-62). Sumi does not specifically state, the reference clock signal generating circuit is a delayed locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals. The examiner takes an Official Notice for implementing the reference signal generating means disclosed by Sumi with a delay locked loop (DLL) circuit. It is well know in the art of using DLL circuits for generating a sequence of clock signals (e.g. for synchronization purposes). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use a DLL circuit in order to implement the reference clock signal generating circuit is a delayed locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals. . One of ordinary skill in the art would be motivated to do so in order to generate a plurality of synchronized delayed instances of the input reference clock signal.

Allowable Subject Matter

Claims 3, 5-12, 15, 17, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 3, the prior art of record fails to disclose or suggest the subject matter of claim 2, further including "divider initial reset means for resetting the first divider once alone with an effective transition timing of the first reference clock signal generated from the reference clock signal generating circuit in wait for the start of the output of the output clock signal from the oscillator circuit after powering the clock multiplying PLL circuit, and resetting the j-th dividers corresponding to the remaining second through n-th dividers once alone, respectively, with timing at which the number of pulses of the output clock signal outputted from the oscillator circuit after the resetting of the first divider reaches P_j".

Regarding claim 5, the prior art of record fails to disclose or suggest the subject matter of claim 4, further including "divider initial reset means for resetting the first divider once alone with an effective transition timing of the first reference clock signal generated from the reference clock signal generating circuit in wait for the start of the output of the output clock signal from the oscillator circuit after powering the clock multiplying PLL circuit, and resetting the j-th dividers corresponding to the remaining second through n-th dividers once alone, respectively, with timing at which the number of the pulses of the output clock signal outputted from the oscillator circuit after the resetting of the first divider reaches the M.(j-1)/n".

Regarding claims 7, 8, and 10, the prior art of fails to disclose or suggest the subject matter of claims 1, 2, and 4, wherein multiplying PLL circuit further includes "an up signal adder for adding first through n-th up signals of respective results of comparisons by the first through n-th phase comparators, a down signal adder for

adding first through n-th down signal thereof, a charge pump for inputting the added up signal and the added down signal".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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